Tyrone Marhguy

Computer Engineering — Computer Architecture / RTL / FPGA / ASIC / Verification

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Summary

Computer Engineering student building from transistor-level CMOS and PCB bring-up through RTL/FPGA, formal verification, and ASIC implementation. Built custom CPUs, low-latency Ethernet/ITCH datapaths, SRAM, and upstream EDA fixes.

Education

University of Pennsylvania — Philadelphia, PA

B.S.E. Computer Engineering — *Aug. 2024 – May 2028*

- **Coursework:** Computer Organization & Design, VLSI, Digital Logic, Embedded Systems

Experience

Hardware & Firmware Engineer — May 2026 – Aug. 2026

Vero Electric — *Philadelphia, PA*

- Developed **embedded C/C++** fault-detection firmware and a **BQ79616 16-channel battery-monitoring front end** for a **240 kWh / 120 kW** system; closed PCB ERC with **0 errors** and debugged bring-up with lab instruments.

Software Engineer Intern — May 2026 – Aug. 2026

Aragorn AI — *Remote*

- Shipped **production backend services and REST APIs** for AI integrations; resolved cross-service failures blocking releases and hardened service boundaries through architecture/code reviews.

Selected Hardware Projects

Tomato - Custom 32-bit Polymorphic CPU | Website | GitHub — 2026 – Present

- Architected a custom **32-bit CPU** around two programmable LUT3 planes + **8-way carry/flag select** (**524,288 ALU configurations**), a **32,768×32-bit 3R1W target register architecture**, and 512-row control ROM.
- Realized on Artix-7 with **256×32-bit registers**, a Python assembler, and ∼2.3K-line HDMI OS; verified **130B Verilator vectors** + formal 1/8/32-bit proofs; a Sky130 Kogge–Stone variant was **1.27× faster and 28% smaller** than ripple.

Low-Latency FPGA Networking & NASDAQ ITCH | UDP/IP | ITCH — 2026

- Built a 15-file **SystemVerilog RMII/MAC/IPv4/UDP stack** with 50/100 MHz CDC; closed at **100 MHz** (WNS +1.985 ns) in **756 LUTs / 599 FFs**, with **20 ns** simulated payload latency.
- Designed an RTL **NASDAQ ITCH parser + 512-slot BRAM order book**: 30 ns parsing and **60 ns Add-to-BBO**; a Python/cocotb golden model drove a **10M-message Verilator regression with zero BBO mismatches**.

8-bit Hybrid ALU - Discrete CMOS + 74HC Logic | GitHub — 2026

- Designed and fabricated a **270×270 mm 8-bit ALU** with **624 discrete MOSFETs + 46 74HC ICs** implementing 19 operations; SPICE-validated transistor gates and exhaustively checked **1.245M input/op combinations** in the behavioral reference flow.

BFloat16 MAC - Sky130 ML Datapath | GitHub — 2025 – 2026

- Designed a **2-stage BF16 multiply → FP32 accumulate** pipeline targeting **50 MHz on Sky130**; verified 1,000 randomized cocotb vectors against a Python golden model and built the **LibreLane/OpenLane hardening flow**.

16×4 Full-Custom SRAM - 22 nm HP | GitHub — 2026

- Designed transistor-level **6T SRAM** with a clocked **StrongARM sense amplifier** and replica-bitline timing; automated NGSpice sweeps and achieved simulated functional readback to **4.571 GHz**.

Open-Source EDA

OpenROAD, Verilator, LibreLane, OpenFPGA | C++ / Python / EDA Infrastructure — 2026

- Merged upstream C++/Python fixes to production EDA tools: repaired an **OpenROAD LEF58/ODB parser**, corrected **Verilator** Linux peak-memory accounting, and restored **LibreLane/Yosys** compatibility/reporting; LibreLane fixes shipped in releases.

Technical Skills

Architecture / RTL: SystemVerilog/Verilog, VHDL, CPU/SoC microarchitecture, pipelining, ISA/datapath design, memory systems, CDC

Verification / Implementation: UVM, SVA, cocotb, formal, Verilator; Vivado, Yosys, OpenROAD, LibreLane/OpenLane, Sky130, KiCad, Electric VLSI, synthesis, STA, P&R, DRC/LVS, SPICE

Programming / Interfaces: Python, C/C++, Embedded C, Tcl, Bash, Linux; Ethernet/RMII/IPv4/UDP, UART, SPI, I^2C